

# REPLICA NETWORK FOR LINEARIZING SWITCHED CAPACITOR CIRCUITS

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## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims the benefit of U.S. Provisional Application No. 60/260,924, filed January 11, 2001.

## BACKGROUND OF THE INVENTION

### Field of the Invention

**[0002]** The present invention relates to a replica network for linearizing switched capacitor circuits.

### Background Art

**[0003]** Switched capacitor sampling networks are commonly used in signal processing applications. They can be efficiently implemented using CMOS technology and are easily integrated with other networks. Among other functions, switched capacitor sampling networks are used for filtering, sample and hold, analog-to-digital conversion, and digital-to-analog conversion.

**[0004]** High performance switch capacitor sampling networks are typically configured as differential circuits. As compared with single-ended designs, a differential embodiment enjoys improved power supply noise rejection, double the output range, and cancellation of even-order distortion components.

**[0005]** FIG. 1A is a schematic diagram of a typical differential switched capacitor sampling network 100. In FIG. 1A, network 100 comprises eight switches:  $S_1$  102,  $S_2$  104,  $S_3$  106,  $S_4$  108,  $S_5$  110,  $S_6$  112,  $S_7$  114, and  $S_8$  116. Collectively,  $S_1$

102,  $S_2$  104,  $S_3$  106, and  $S_4$  108 are referred to as signal conducting switches, while  $S_5$  110,  $S_6$  112,  $S_7$  114, and  $S_8$  116 are collectively referred to as summing junction switches.

[0006] FIG. 1B illustrates a two-phase nonoverlapping clock scheme 118 defined by four clock waveforms:  $\phi_1$  120,  $\phi_{1D}$  122,  $\phi_2$  124, and  $\phi_{2D}$  126. The position of each switch at any given time is determined by its corresponding clock waveform. In a representative embodiment, a switch is open when its corresponding clock waveform is "off" and closed when its corresponding clock waveform is "on." One skilled in the art would recognize that network 100 could be configured with other relationships between the state of the switches and their corresponding clock waveforms.

[0007] Clock scheme 118 is configured so that  $\phi_1$  120 and  $\phi_{1D}$  122 are on when  $\phi_2$  124 and  $\phi_{2D}$  126 are off. Clock waveforms  $\phi_{1D}$  122 and  $\phi_{2D}$  126 are similar to, respectively, clock waveforms  $\phi_1$  120 and  $\phi_2$  124. However, the falling edges of  $\phi_{1D}$  122 and  $\phi_{2D}$  126 are not initiated until after  $\phi_1$  120 and  $\phi_2$  124 have returned to their "off" states. Together, clock waveforms  $\phi_1$  120 and  $\phi_{1D}$  122 define a sampling phase of clock scheme 118 while clock waveforms  $\phi_2$  124 and  $\phi_{2D}$  126 define a transferring phase.

[0008] Network 100 further comprises a positive voltage sampling capacitor  $C_1^+$  128, a negative voltage sampling capacitor  $C_1^-$  130, and a differential integrator 132. Differential integrator 132 comprises an operational amplifier 134 with an inverting terminal  $T^-$  136, a noninverting terminal  $T^+$  138, a positive voltage output signal  $V_o^+$  140, and a negative voltage output signal  $V_o^-$  142. A positive voltage feedback capacitor  $C_2^+$  144 is connected in parallel with operational amplifier 134 between  $T^-$  136 and  $V_o^+$  140. A negative voltage feedback capacitor  $C_2^-$  146 is connected in parallel with operational amplifier 134 between  $T^+$  138 and  $V_o^-$  142. Both a positive voltage input signal  $V_i^+$  146 and a negative voltage input signal  $V_i^-$  148 are received by network 100.

[0009] Switch  $S_1$  102 is disposed between  $V_i^+$  146 and  $C_1^+$  128. Switch  $S_2$  104 is disposed between  $V_i^-$  148 and  $C_1^+$  128, such that  $S_1$  102 and  $S_2$  104 are

connected in parallel with each other at a node  $N_1$  150 upstream of  $C_1^+$  128. Switch  $S_3$  106 is disposed between  $V_i^+$  146 and  $C_1^-$  130. Switch  $S_4$  108 is disposed between  $V_i^-$  148 and  $C_1^-$  130, such that  $S_3$  106 and  $S_4$  108 are connected in parallel with each other at a node  $N_2$  152 upstream of  $C_1^-$  130.

[0010] Switch  $S_5$  110 is disposed between a node  $N_3$  154 downstream of  $C_1^+$  128 and  $T^-$  136. Switch  $S_6$  112 is disposed between  $N_3$  154 and an analog ground connection 156. Switch  $S_7$  114 is disposed between a node  $N_4$  158 downstream of  $C_1^-$  130 and  $T^+$  138. Switch  $S_8$  116 is disposed between  $N_4$  158 and analog ground connection 156.

[0011] Operation of network 100 can be explained by tracing the circuits that are established in response to the cycling of the clock waveforms of clock scheme 118.

[0012] At a time  $t_0$ , clock waveforms  $\phi_1$  120 and  $\phi_{1D}$  122 cycle to the on state while clock waveforms  $\phi_2$  124 and  $\phi_{2D}$  126 remain in the off state. In response to the on state of  $\phi_1$  120, switches  $S_6$  112 and  $S_8$  116 close. In response to the on state of  $\phi_{1D}$  122, switches  $S_1$  102 and  $S_4$  108 close. With  $S_1$  102 and  $S_6$  112 closed, a circuit is established between  $V_i^+$  146 and analog ground 156 through  $C_1^+$  128. This circuit allows  $V_i^+$  146 to be sampled as a charge on an upstream plate  $P_{1u}^+$  160 of  $C_1^+$  128. The value of this charge is equal to the product of the capacitance of  $C_1^+$  128 and the voltage of  $V_i^+$  146. Likewise, with  $S_4$  108 and  $S_8$  116 closed, a circuit is established between  $V_i^-$  148 and analog ground 156 through  $C_1^-$  130. This circuit allows  $V_i^-$  148 to be sampled as a charge on an upstream plate  $P_{1u}^-$  162 of  $C_1^-$  130. The value of this charge is equal to the product of the capacitance of  $C_1^-$  130 and the voltage of  $V_i^-$  148.

[0013] At a time  $t_1$ , clock waveform  $\phi_1$  120 cycles to the off state, while  $\phi_{1D}$  122 remains in the on state. Clock waveforms  $\phi_2$  124 and  $\phi_{2D}$  126 remain in the off state. In response to the off state of  $\phi_1$  120, switches  $S_6$  112 and  $S_8$  116 open. Opening switch  $S_6$  112 breaks the circuit between  $V_i^+$  146 and analog ground 156. This isolates the charge stored on upstream plate  $P_{1u}^+$  160, thus effectively sampling  $V_i^+$  146. Likewise, opening switch  $S_8$  116 breaks the circuit between  $V_i^-$

148 and analog ground 156. This isolates the charge stored on upstream plate  $P_{lu}^-$  162, thus effectively sampling  $V_i^-$  148.

[0014] At a time  $t_2$ , clock waveform  $\phi_{ID}$  122 cycles to the off state. Clock waveforms  $\phi_1$  120,  $\phi_2$  124, and  $\phi_{2D}$  126 remain in the off state. In response to the off state of  $\phi_{ID}$  122, switches  $S_1$  102 and  $S_4$  108 open. By delaying the opening of switches  $S_1$  102 and  $S_4$  108 until after switches  $S_6$  112 and  $S_8$  116 have been opened, and thus isolating the charges stored on  $C_1^+$  128 and  $C_1^-$  130, the sampled signals are unaffected by the charge injection that occur after switches  $S_6$  112 and  $S_8$  116 have been opened. Particularly, the sampled signals are not distorted by any charge injection resulting from the opening of switches  $S_1$  102 and  $S_4$  108.

[0015] At a time  $t_3$ , clock waveforms  $\phi_2$  124 and  $\phi_{2D}$  126 cycle to the on state while clock waveforms  $\phi_1$  120 and  $\phi_{ID}$  122 remain in the off state. In response to the on state of  $\phi_2$  124, switches  $S_5$  110 and  $S_7$  114 close. In response to the on state of  $\phi_{2D}$  126, switches  $S_2$  104 and  $S_3$  106 close. With  $S_2$  104 and  $S_5$  110 closed, a circuit is established between  $V_i^-$  148 and differential integrator 132 through  $C_1^+$  128. This circuit enables the charge on upstream plate  $P_{lu}^+$  160 to be transferred to differential integrator 132. One skilled in the art would recognize that the transferred charge is defined by Eq. (1):

$$\text{Eq. (1) } Q = C_s \times [V_i^+ - V_i^-],$$

where  $C_s$  equals the value of the capacitance of  $C_1^+$  128. As it is desired that the charge transferred to differential integrator 132 equals the charge stored on capacitor  $C_1^+$  128, the use of a differential circuit enables  $C_1^+$  128 to have a smaller value of capacitance than it would have in a single-ended switched capacitor integrator configuration having the same gain and the same value of capacitance for the feedback capacitor. Advantageously, a smaller value for  $C_1^+$  128: (1) increases the speed of network 100, (2) reduces the degradation in bandwidth of frequencies that network 100 can support, and (3) enables the feedback factor of differential integrator 132 to be nearer to unity, where feedback factor is defined by Eq. (2):

$$\text{Eq. (2) Feedback Factor} = C_f / [C_f + C_s].$$

- [0016] Likewise, with  $S_3$  106 and  $S_7$  114 closed, a circuit is established between  $V_i^+$  146 and differential integrator 132 through  $C_1^-$  130. This circuit enables the charge on upstream plate  $P_{1u}^-$  162 to be transferred to differential integrator 132 in the same manner as described above.
- [0017] At a time  $t_4$ , clock waveform  $\phi_2$  124 cycles to the off state, while  $\phi_{2D}$  126 remains in the on state. Clock waveforms  $\phi_1$  120 and  $\phi_2$  122 remain in the off state. In response to the off state of  $\phi_2$  124, switches  $S_5$  110 and  $S_7$  114 open. Opening switch  $S_5$  110 breaks the circuit between  $V_i^-$  148 and differential integrator 132. This isolates the charge transferred to differential integrator 132 from  $C_1^+$  128. Likewise, opening switch  $S_7$  114 breaks the circuit between  $V_i^+$  146 and differential integrator 132. This isolates the charge transferred to differential integrator 132 from  $C_1^-$  130.
- [0018] At a time  $t_5$ , clock waveform  $\phi_{2D}$  126 cycles to the off state. Clock waveforms  $\phi_1$  120,  $\phi_2$  122, and  $\phi_2$  124 remain in the off state. In response to the off state of  $\phi_{2D}$  126, switches  $S_2$  104 and  $S_3$  106 open. By delaying the opening of switches  $S_2$  104 and  $S_3$  106 until after switches  $S_5$  110 and  $S_7$  114 have been opened, the transferred signals are unaffected by the charge injection that occur after switches  $S_5$  110 and  $S_7$  114 have been opened. Particularly, the transferred signals are not distorted by any charge injection resulting from the opening of switches  $S_2$  104 and  $S_3$  106.
- [0019] At a time  $t_6$ , clock waveforms  $\phi_1$  120 and  $\phi_{1D}$  122 cycle to the on state while clock waveforms  $\phi_2$  124 and  $\phi_{2D}$  126 remain in the off state. The response of network 100 to the on state of  $\phi_1$  120 and  $\phi_{1D}$  122 is identical to the response to the on state at time  $t_0$  as explained above. Likewise, at times subsequent to  $t_6$ , network 100 operates in the manner explained above.
- [0020] In a more typical embodiment, the switches of FIG. 1A are implemented with MOSFETs. FIG. 2 is a schematic diagram of a differential switched capacitor sampling network 200, with MOSFET switches. This circuit is described in Stephen R. Norsworthy *et al.*, *Delta-Sigma Data Converters*:

*Theory, Design, and Simulation*, The Institute of Electrical and Electronics Engineers, Inc. 1997, which is incorporated herein by reference.

[0021] In FIG. 2, signal conducting switches  $S_1$  202,  $S_2$  204,  $S_3$  206, and  $S_4$  208 are implemented with CMOSFETs, while summing junction switches  $S_5$  210,  $S_6$  212,  $S_7$  214, and  $S_8$  216 are implemented with NMOSFETs. However, one skilled in the art would recognize that the type of MOSFETs used to implement the switches would be a function of, among other considerations, the signal environment in which network 200 would operate. The use of CMOSFETs for the signal conducting switches extends the range of voltages over which the signal conducting switches would conduct. The use of CMOSFETs for this particular purpose is well understood in the art.

[0022] For each MOSFET switch of FIG. 2, the signal path is between its source and drain terminals. The state of the MOSFET switch is controlled by a clock waveform applied to its gate terminal. For the PMOSFET portion of a CMOSFET, the clock waveform is opposite of the clock waveform used for the NMOSFET portion. Thus, a clock waveform  $\phi_{1D}$  [bar] 218 is in the on state when clock waveform  $\phi_{1D}$  122 is in the off state and vice versa. Likewise, a clock waveform  $\phi_{2D}$  [bar] 220 is in the on state when clock waveform  $\phi_{2D}$  126 is in the off state and vice versa.

[0023] While delaying the opening of the signal conducting switches until after the summing junction switches have been opened isolates the sampled signal from distortions due to charge injections from the signal conducting switches, this clock scheme does not protect the sampled signal from distortions due to: (1) variations in the resistances of the signal conducting switches that operate in an environment of a varying voltage signal, or (2) charge injections from the summing junction switches.

[0024] Where a switch in a differential switched capacitor sampling network is implemented as a MOSFET, the resistance of the switch is defined by Eq. (3):

$$\text{Eq. (3) } R = 1/[k \times (V_{GS} - V_T - V_{DS})],$$

where  $k$  is a constant,  $V_{GS}$  is the voltage potential between the gate and source terminals,  $V_T$  is the threshold voltage, and  $V_{DS}$  is the voltage potential between the drain and source terminals of the MOSFET. These parameters are well understood in the art.

[0025] Applying Eq. (3) to a signal conducting MOSFET switch of FIG. 2, the skilled artisan will appreciate that when the signal conducting MOSFET switch (e.g.,  $S_1$  202,  $S_2$  204,  $S_3$  206, or  $S_4$  208) is on, a signal with a varying voltage is applied to the source terminal, while a constant voltage (i.e., the clock) is applied to the gate terminal. This produces a voltage  $V_{GS}$  that varies in a signal dependent manner. This, in turn, results in the MOSFET switch having a resistance  $R$  whose value is signal dependent. As resistance  $R$  of the MOSFET switch varies, the drop in the voltage potential of the signal across the switch also changes. Changes in this drop in voltage distort the voltage potential of the signal that is sampled by a sampling capacitor. The distortion is signal dependent. This phenomenon is referred to as track mode distortion.

[0026] Meanwhile, delaying the opening of a signal conducting switch during the transferring phase (e.g.,  $S_2$  204 or  $S_3$  206) until after its corresponding summing junction switch connected to the differential integrator (e.g.,  $S_5$  210 or  $S_7$  214) has been opened exposes the transferred signal to distortions from charge injections from the summing junction switch connected to the differential integrator. Specifically, as the summing junction switch connected to the differential integrator is opened, a residual charge retained on it will have two paths through which to dissipate: (1) from the summing junction switch, through the sampling capacitor and the signal conducting switch, and towards the signal, and (2) from the summing junction switch towards the differential integrator.

[0027] The total residual charge will divide between these two paths according to the resistance that each path presents. From FIGS. 1A, 1B, and 2, it can be observed that at  $t_4$  the signal conducting MOSFET switch (e.g.,  $S_2$  202 or  $S_3$  206) is closed while the summing junction MOSFET switch (e.g.,  $S_5$  210 or  $S_7$  214) is being opened. As explained above, the resistance  $R$  of the closed signal

conducting MOSFET switch is signal dependent. Therefore, the amount of the total residual charge that dissipates through the closed signal conducting MOSFET switch will also be signal dependent. Because the amount of the total residual charge that dissipates towards the differential integrator is the difference between the total residual charge and the amount of the total residual charge that dissipates through the closed signal conducting MOSFET switch, the amount of the total residual charge that dissipates towards the differential integrator will also be signal dependent and distort the signal transferred to the differential integrator.

**[0028]** Previous efforts to correct for signal dependent distortion in differential switched capacitor sampling networks have used midrange threshold voltage (about 0.3 volts) MOSFET switches. Differential switched capacitor sampling networks using these devices have been shown to reduce distortion. However, fabrication of these MOSFET switches requires the use of expensive extra mask layers. Also, at larger voltage input signal amplitudes and at higher voltage input signal frequencies, this approach has been shown to be ineffective at reducing signal distortion.

**[0029]** Alternatively, bootstrap capacitors have been used to buffer against changes in voltage between the gate and source terminals of signal conducting MOSFET switches. FIG. 3 is a schematic diagram of a signal conducting MOSFET switch 300 with a bootstrap capacitor 302 connected between a gate terminal 304 and a source terminal 306. During the on state of the clock waveform, bootstrap capacitor 302 acts to maintain  $V_{GS}$  at a relatively constant voltage. As can be seen by applying Eq. (3), this mitigates the variation in the resistance  $R$  of signal conducting MOSFET switch 300 and thus reduces the degree of signal dependent distortion. During the off state of the clock waveform, bootstrap capacitor 302 is connected between a voltage source 308 and ground 310. This is done so that bootstrap capacitor 302 can be charged by voltage source 308 to enable it to perform its function during the on state of the clock waveform.



[0030] While the use of bootstrap capacitors has proven to be an adequate solution in many applications, it does present several disadvantages. Specifically, the bootstrap capacitors must be relatively large (on an order of magnitude that is four to five times the capacitance between the gate and source terminals of the signal conducting MOSFET switches) and they consume a relatively large amount of power. Furthermore, of the three parameters that determine the resistance  $R$  of the signal conducting MOSFET switches –  $V_{GS}$ ,  $V_T$ , and  $V_{DS}$  – the use of bootstrap capacitors essentially addresses only one of these factors:  $V_{GS}$ . This limits the accuracy of this solution for use in high precision applications. What is needed is a mechanism that controls the resistance  $R$  of a signal conducting MOSFET switch so that the resistance  $R$  is independent of the signal voltage and the switched capacitor circuit is linearized.

#### BRIEF SUMMARY OF THE INVENTION

[0031] The present invention relates to a replica network for linearizing switched capacitor circuits. A bridge circuit with a MOSFET resistor disposed in a resistor branch of the bridge circuit is provided. A noninverting terminal of an operational amplifier is connected to a first node of the bridge circuit and an inverting terminal of the operational amplifier is connected to a second node of the bridge circuit. The second node is separated from the first node by a third node of the bridge circuit. An output of the operational amplifier is provided to a gate terminal of the MOSFET resistor and to the gate terminal of the MOSFET switch, thereby controlling the voltage to the gate terminal of the MOSFET switch.

[0032] In an embodiment, a compensation capacitor is connected in parallel between the output and the second node. In another embodiment, an analog ground is connected to a third node of the bridge circuit. In yet another embodiment, a voltage input signal is connected to a fourth node of the bridge circuit.

**[0033]** Preferably, the resistance of a first resistor connected between the first node and the third node equals the resistance of a second resistor connected between the second node and the third node. Preferably, the MOSFET resistor is connected between the second node and the fourth node. Preferably, the resistance of a third resistor connected between the first node and the fourth node is smaller than the resistance of the first resistor or the second resistor.

**[0034]** In an embodiment, the output of the operational amplifier controls the resistance of the MOSFET resistor so that the resistance of the MOSFET resistor equals the resistance of the third resistor. In another embodiment, the output of the operational amplifier controls the resistance of the MOSFET switch so that the resistance of the MOSFET switch equals the resistance of the third resistor. Preferably, the MOSFET resistor is the same type and size as the MOSFET switch. Preferably, the MOSFET resistor has a threshold voltage less than or equal to zero volts. Advantageously, MOSFETs with threshold voltages at this level are inexpensive to fabricate. In an embodiment, the MOSFET resistor is a native NMOSFET device.

**[0035]** In an embodiment, a first switch is disposed within the connection between the output and the gate terminal of the MOSFET switch. In a related embodiment, the first switch cycles to an open state and a closed state in response to an on state and an off state of a first clock waveform. In another related embodiment, a second switch is connected between a fifth node and analog ground. The fifth node is disposed within the connection between the first switch and the gate terminal of the MOSFET switch. In yet another related embodiment, the second switch cycles to an open state and a closed state in response to an on state and an off state of a second clock waveform.

**[0036]** In an embodiment, the replica network comprises two replica networks. In a related embodiment, each replica network receives a voltage input signal from a differential circuit. In another related embodiment, the differential circuit is a differential switched capacitor sampling network.

**[0037]** Unlike the use of a bootstrap capacitor, which acts to maintain  $V_{GS}$  of a MOSFET switch at a relatively constant voltage and thus mitigates the variation in the resistance of the MOSFET switch, the replica network of the present invention acts to vary  $V_{GS}$  as necessary to peg the resistances  $R$  of the MOSFET switch to the fixed resistance value of resistor in the bridge circuit.

**[0038]** In this manner, the replica network of the present invention provides a mechanism that controls the resistance of the MOSFET switch so that it is independent of the signal voltage. For a differential switched capacitor sampling network, this mitigates signal dependent distortion due to charge injection from the summing junction switches during the transferring phase and eliminates track mode distortion due to variations in the resistances of the signal conducting MOSFET switches during the sampling phase. Thus, the replica network of the present invention linearizes the switched capacitor circuit.

#### BRIEF DESCRIPTION OF THE FIGURES

**[0039]** The accompanying drawings, which are incorporated herein and form part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

**[0040]** FIG. 1A is a schematic diagram of a typical differential switched capacitor sampling network 100.

**[0041]** FIG. 1B illustrates a two-phase nonoverlapping clock scheme 118 defined by four clock waveforms.

**[0042]** FIG. 2 is a schematic diagram of a differential switched capacitor sampling network 200, with MOSFET switches.

**[0043]** FIG. 3 is a schematic diagram of a signal conducting MOSFET switch 300 with a bootstrap capacitor 302 connected between a gate terminal 304 and a source terminal 306.

- [0044] FIG. 4 is a schematic diagram of a replica network 400 that adjusts the clock voltage to the gate terminal of each signal conducting MOSFET switch so that the resistance  $R$  is independent of the signal voltage.
- [0045] FIG. 5 shows a flow chart of a method 500 for reducing track mode distortion in a switched capacitor circuit.
- [0046] FIG. 6 shows a flow chart of a method 600 of regulating the gate voltage of a MOSFET resistor disposed in a resistor branch of the bridge circuit.
- [0047] The preferred embodiments of the invention are described with reference to the figures where like reference numbers indicate identical or functionally similar elements. Also in the figures, the left most digit of each reference number identifies the figure in which the reference number is first used.

#### DETAILED DESCRIPTION OF THE INVENTION

- [0048] The present invention relates to a replica network for linearizing switched capacitor circuits. FIG. 4 is a schematic diagram of a replica network 400 that adjusts the clock voltage to the gate terminal of each signal conducting MOSFET switch so that the resistance  $R$  is independent of the signal voltage. Replica network 400 comprises a positive voltage input signal network 402, which receives positive voltage input signal  $V_i^+$  146, and a negative voltage input signal network 404, which receives negative voltage input signal  $V_i^-$  148. Each voltage input signal network 402, 404 comprises a bridge circuit 406 and an operational amplifier 408.
- [0049] Each bridge circuit 406 comprises four resistance branches connected between four nodes. A resistor  $R_1$  410 is connected between a node A 412 and a node B 414. A resistor  $R_2$  416 is connected between node B 414 and a node C 418. A resistor  $R_3$  420 is connected between node C 418 and a node D 422. A MOSFET resistor 424 is connected between node D 422 and node A 412. Resistors  $R_2$  416 and  $R_3$  420 have the same value of resistance. Preferably, the resistance value of resistors  $R_2$  416 and  $R_3$  420 is larger than the resistance value

420a,b is larger than the resistance value of resistor  $R_1$  410a,b. In an embodiment, MOSFET resistor 424a,b has a threshold voltage less than or equal to zero volts. Advantageously, MOSFETs with threshold voltages at this level are inexpensive to fabricate. Furthermore, MOSFET resistor 424a,b should be of the same type and size as the signal conducting MOSFET switches shown in FIG. 2. MOSFET resistor 424a,b could be, but is not limited to, a CMOSFET, a NMOSFET, or a PMOSFET, as would be understood by one skilled in the art. Particularly, MOSFET resistor 424a,b could be a native NMOSFET device. FIG. 4 shows replica network 400 with a native NMOSFET device used for MOSFET resistor 424a,b and also reproduces differential switched capacitor sampling network of FIGS. 1A and 2 with native NMOSFET devices used for the signal conducting switches.

**[0050]** In FIG. 4, in a representative embodiment, node A 412a,b receives a voltage input signal, node B 414a,b is connected to the noninverting terminal of operational amplifier 408a,b, node C 418a,b is connected to analog ground 156, and node D 422a,b is connected to the inverting terminal of operational amplifier 408a,b. One skilled in the art would recognize other configurations by which the voltage input signal and operational amplifier could be connected to the nodes of bridge circuit 406a,b in the manner of the present invention. Therefore, the present invention is not limited to the configuration shown in FIG. 4.

**[0051]** Each operational amplifier 408a,b, at its output terminal, produces an output voltage 426a,b that is used as the clock voltage for its respective signal conducting MOSFET switches (e.g.,  $S_1$  202,  $S_2$  204,  $S_3$  206, or  $S_4$  208). Output voltage 426a from positive voltage input signal network 402 is used as the clock voltages for signal conducting MOSFET switches  $S_1$  202 and  $S_2$  204, while output voltage 426b from negative voltage input signal network 404 is used as the clock voltages for signal conducting MOSFET switches  $S_3$  206 and  $S_4$  208.

**[0052]** While output voltages 426a,b determine the values of the clock voltages, the shape of the clock waveforms are determined by switches  $S_a$  428,  $S_b$  430,  $S_c$  432,  $S_d$  434,  $S_e$  436,  $S_f$  438,  $S_g$  440, and  $S_h$  442. In an embodiment, these

switches are implemented as MOSFET switches. These are appropriately sized (i.e., much smaller than the signal conducting MOSFET switches) to reduce the second order effect of clock feedthrough onto the sampling capacitors (e.g.,  $C_1^+$  128 and  $C_1^-$  130).

[0053] For signal conducting MOSFET switch  $S_1$  202, the shape of the clock waveform applied to its gate terminal is controlled by switch  $S_a$  428. Switch  $S_a$  428 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{1D}$  122. With switch  $S_a$  428 closed, a circuit is established between operational amplifier 408 and the gate terminal of switch  $S_1$  202. When switch  $S_a$  428 opens, switch  $S_b$  430 closes. Switch  $S_b$  430 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{1D}$  [bar] 218. With switch  $S_b$  430 closed, a circuit is established between the gate terminal of switch  $S_1$  202 and analog ground 156. This enables any residual charge on the gate terminal of switch  $S_1$  202 to dissipate to analog ground 156 so that switch  $S_1$  202 opens in a timely manner.

[0054] In a similar manner, switch  $S_c$  432 controls the shape of the clock waveform applied to the gate terminal of signal conducting MOSFET switch  $S_2$  204. Switch  $S_c$  432 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{2D}$  126. Switch  $S_d$  434 dissipates any residual charge on the gate terminal of switch  $S_2$  204 to analog ground 156. Switch  $S_d$  434 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{2D}$  [bar] 220.

[0055] Likewise, switch  $S_e$  436 controls the shape of the clock waveform applied to the gate terminal of signal conducting MOSFET switch  $S_3$  206. Switch  $S_e$  436 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{1D}$  122. Switch  $S_f$  438 dissipates any residual charge on the gate terminal of switch  $S_3$  206 to analog ground 156. Switch  $S_f$  438 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{1D}$  [bar] 218.

cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{2D}$  126. Switch  $S_h$  442 dissipates any residual charge on the gate terminal of switch  $S_4$  208 to analog ground 156. Switch  $S_h$  442 cycles open and closed in response, respectively, to the off and on states of clock waveform  $\phi_{2D}$  [bar] 220.

[0057] Each voltage input signal network 402, 404 receives its respective voltage input signal (i.e.,  $V_i^+$  146 or  $V_i^-$  148) at node A 412. Variation in the voltage input signal causes the resistance  $R$  of MOSFET resistor 424 to vary in the manner described above. This, in turn, causes the voltage measurements at node B 414 and node D 422 to be unequal. Operational amplifier 408 responds to these unequal inputs to change output voltage 426. Output voltage 426 is proportional to the difference between the voltage of node B 414 and the voltage of node D 422. Output voltage 426 is applied as feedback to the gate terminal of MOSFET resistor 424, thus changing the value of  $V_G$  of MOSFET resistor 424. The feedback network is designed to maintain the resistance  $R$  of MOSFET resistor 424 equal to the value of resistor  $R_1$  410, so that bridge circuit 406 remains in balance. Thus, the feedback network is designed so that changes to the value of  $V_G$  cause, through application of Eq. (3), appropriate changes to the value of  $V_{GS}$  so that the resistance  $R$  of MOSFET resistor 424 is maintained equal to the value of resistor  $R_1$  410.

[0058] In an embodiment, a compensation capacitor  $C_{comp}$  444 is connected in parallel between node D 422 and the output of operational amplifier 408. Compensation capacitor  $C_{comp}$  444 is a feedforward shunt capacitor that improves the stability of the feedback network between operational amplifier 408 and bridge circuit 406. One skilled in the art will understand that the feedback network has a process and temperature dependent feedback factor due to the transconductance of the triode region of MOSFET resistor 424. The process and temperature dependent feedback factor changes the effective bandwidth of the feedback network with respect to process and operating temperature. This degrades the gain of the feedback network. The phase margin, and therefore the

bandwidth of the feedback network with respect to process and operating temperature. This degrades the gain of the feedback network. The phase margin, and therefore the stability, of the feedback network is also effected by the process and operating temperature. Compensation capacitor  $C_{comp}$  444a,b provides lead compensation and ensures sufficient phase margin over process variations.

[0059] In an embodiment, operational amplifier 408a,b has a folded cascode topology to support a large bandwidth and high gain in the presence of low feedback factors. Operational amplifier 408a,b needs to maintain sufficient feedback network gain at high frequencies. There is a direct relation between the amount of linearization that can be obtained and the amount of power consumed. Greater bandwidth in the feedback network can be obtained at a cost of additional power dissipation.

[0060] Where MOSFET resistor 424a,b is maintained sufficiently in triode, with  $V_{DS}$  less than the difference between  $V_{GS}$  and  $V_T$ , the resistance  $R$  of MOSFET switches  $S_1$  202,  $S_2$  204,  $S_3$  206, and  $S_4$  208 will track the value of resistor  $R_1$  410a,b. Preferably, MOSFET resistor 424a,b has a threshold voltage less than or equal to zero volts.

[0061] As noted above, MOSFET resistor 424a,b should be of the same type and size as the signal conducting MOSFET switches whose clock voltages MOSFET resistor 424a,b regulates. So, for positive voltage input signal network 402, MOSFET resistor 424a should be of the same type and size as signal conducting MOSFET switches  $S_1$  202 and  $S_2$  204, while for negative voltage input signal network 404, MOSFET resistor 424b should be of the same type and size as signal conducting MOSFET switches  $S_3$  206 and  $S_4$  208.

[0062] As can be observed in FIG. 4, because: (1) the signal conducting MOSFET switches (i.e.,  $S_1$  202,  $S_2$  204,  $S_3$  206, and  $S_4$  204) are of the same type and size as their corresponding MOSFET resistors 424a,b, (2) identical voltage values are applied to the gate terminals of the signal conducting MOSFET switches and their corresponding MOSFET resistors 424a,b, and (3) the same voltage input signals (i.e.,  $V_i^+$  146 and  $V_i^-$  148) are applied to both the differential



switched capacitor sampling network and replica network 400, the resistances  $R$  of the signal conducting MOSFET switches will also be held to values near the value of resistor  $R_1$  410a,b.

[0063] Unlike the use of bootstrap capacitors, which act to maintain  $V_{GS}$  at a relatively constant voltage and thus mitigate the variation in the resistances  $R$  of the signal conducting MOSFET switches, replica network 400 acts to vary  $V_{GS}$  only as much as necessary to peg the resistances  $R$  of the signal conducting MOSFET switches  $S_1$  202,  $S_2$  204,  $S_3$  206, and  $S_4$  204 to the fixed resistance value of resistor  $R_1$  410a,b in response to the changes in threshold voltage of MOSFET resistor 424a,b with respect to varying input signal voltages. In this manner, replica network 400 provides a mechanism that controls the resistances  $R$  of the signal conducting MOSFET switches so that they are independent of the signal voltage. This, in turn: (1) mitigates signal dependent distortion due to charge injection from the summing junction switches (e.g.,  $S_5$  110 and  $S_7$  114) during the transferring phase and (2) eliminates track mode distortion due to variations in resistance  $R$  of the signal conducting MOSFET switches (e.g.,  $S_1$  202 and  $S_4$  208) during the sampling phase. Thus, the switched capacitor circuit is linearize.

[0064] Although replica network 400 has been described above for use in maintaining the resistances  $R$  of signal conducting MOSFET switches in a differential switched capacitor sampling network application, one skilled in the art will recognize other applications for replica network 400. Therefore, the present invention should not be limited to differential switched capacitor sampling network applications.

[0065] FIG. 5 shows a flow chart of a method 500 for reducing track mode distortion in a switched capacitor circuit. One skilled in the art will recognize that there are several means by which the steps of method 500 can be realized.

[0066] In method 500, at a step 502, a voltage input signal is connected to a first node of a bridge circuit (e.g., 400) and to the switched capacitor circuit (e.g., 200). At a step 504, a gate voltage of a MOSFET resistor (e.g., 424a,b) disposed

in a resistor branch of the bridge circuit is regulated to control the resistance of the MOSFET resistor. Further to explain step 504, FIG. 6 shows a flow chart of a method 600 of regulating the gate voltage of a MOSFET resistor disposed in a resistor branch of the bridge circuit.

**[0067]** In method 600, at a step 602, a noninverting terminal of an operational amplifier (e.g., 408a,b) is connected to a second node of the bridge circuit and an inverting terminal of the operational amplifier is connected to a third node of the bridge circuit. The third node is separated from the second node by the first node of the bridge circuit. At a step 604, an output of the operational amplifier is connected to a gate terminal of the MOSFET resistor, thereby regulating the gate voltage of the MOSFET resistor disposed in the resistance branch of the bridge circuit to control the resistance of the MOSFET resistor. Preferably, a compensation capacitor is connected in parallel between the output of the operational amplifier and the third node.

**[0068]** Preferably, the MOSFET resistor is connected between the first node and the third node. In a related embodiment, the output of the operational amplifier controls the resistance of the MOSFET resistor so that the resistance of the MOSFET resistor equals the resistance of a resistor connected between the first node and the second node.

**[0069]** Returning to FIG. 5, in method 500, at a step 506, the regulated gate voltage is connected to a gate terminal of a signal conducting MOSFET switch (e.g., 202, 204, 206, or 208) in the switched capacitor circuit, thereby controlling the resistance of the signal conducting MOSFET switch so that it is independent of the voltage input signal, thereby reducing the track mode distortion in the switched capacitor circuit. Preferably, the MOSFET resistor is the same type and size as the signal conducting MOSFET switch.

**[0070]** In an embodiment in which the gate voltage of a MOSFET resistor is regulated as prescribed by method 600, preferably, the output of the operational amplifier controls the resistance of the signal conducting MOSFET switch so that

the resistance of the signal conducting MOSFET switch equals the resistance of a resistor connected between the first node and the second node.

**[0071]** Alternatively, method 500 can be used to reduce signal distortion due to charge injection from a summing junction switch in a switched capacitor circuit.

#### Conclusion

**[0072]** While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.